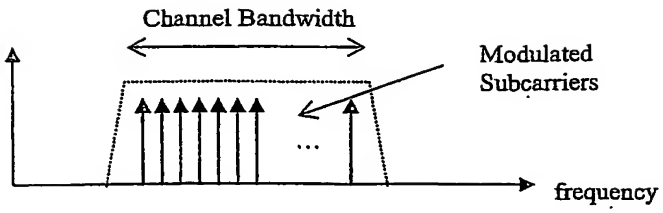

Figure 1

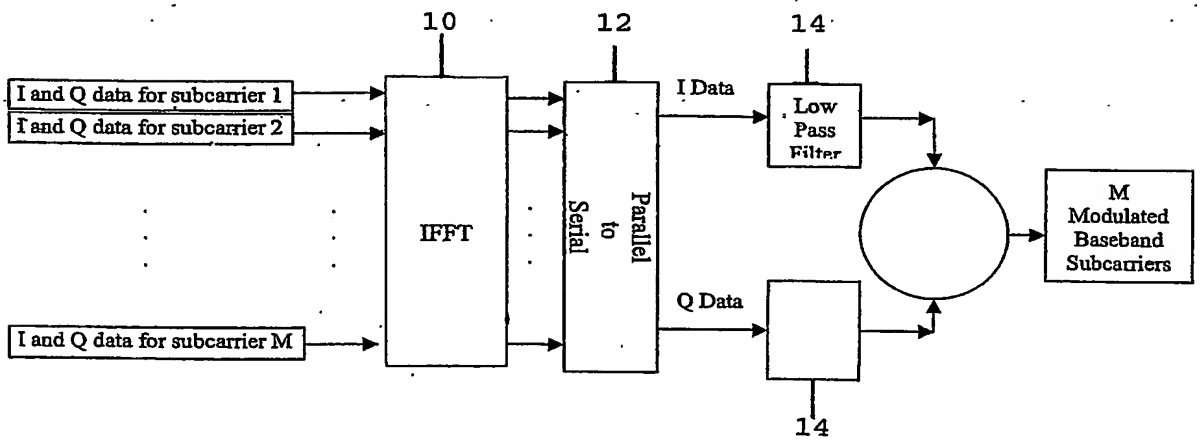

Figure 2

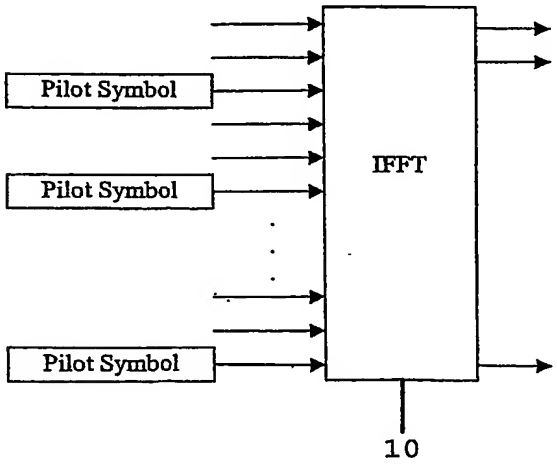

Figure 3

Normal Block S_1	Reciprocal Block S_2

Figure 4

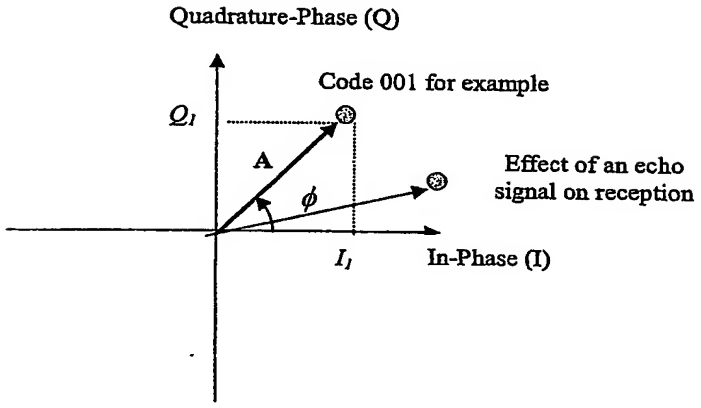

Figure 5

Data 1	Data 2	...	Data k	...	Data (N-1)	Data N

Figure 6

Data Block 1

$$\begin{bmatrix} A_{110}\exp(j(\phi_{110}+\phi_{k10})) \\ A_{120}\exp(j(\phi_{120}+\phi_{k20})) \\ . \\ . \\ . \\ A_{1M0}\exp(j(\phi_{1M0}+\phi_{kM0})) \end{bmatrix}$$

Data Block 2

$$\begin{bmatrix} A_{210}\exp(j(\phi_{210}+\phi_{k10})) \\ A_{220}\exp(j(\phi_{220}+\phi_{k20})) \\ . \\ . \\ . \\ A_{2M0}\exp(j(\phi_{2M0}+\phi_{kM0})) \end{bmatrix} \quad \cdots$$

Pilot Control Data Block k

$$\begin{bmatrix} A_{k10}\exp(j\phi_{k10}) \\ A_{k20}\exp(j\phi_{k20}) \\ . \\ . \\ . \\ A_{kM0}\exp(j\phi_{kM0}) \end{bmatrix} \quad \cdots$$

$$\cdots \begin{bmatrix} A_{N10}\exp(j(\phi_{N10}+\phi_{k10})) \\ A_{N20}\exp(j(\phi_{N20}+\phi_{k20})) \\ . \\ . \\ . \\ A_{NM0}\exp(j(\phi_{NM0}+\phi_{kM0})) \end{bmatrix}$$

Data Block N

Figure 7

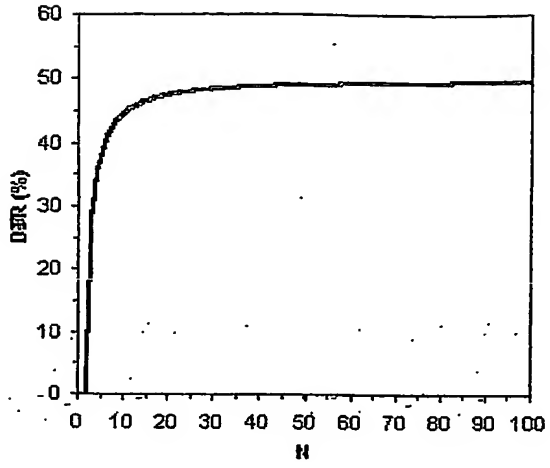

Figure 8

Data 1	Pilot Control Block Data 2	Data3

Figure 9

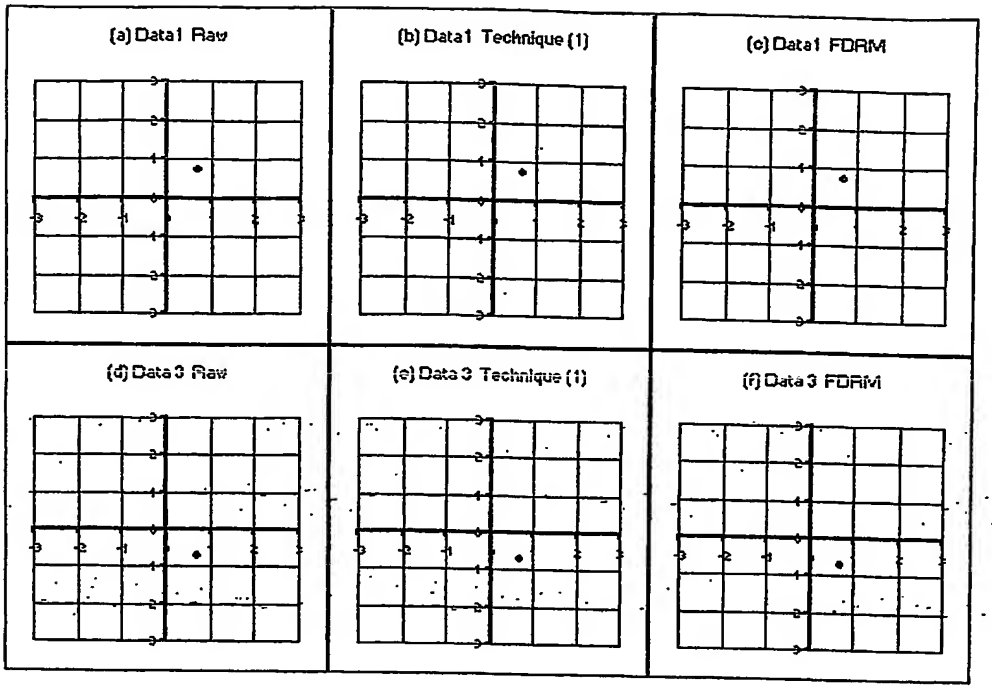

Figure 10

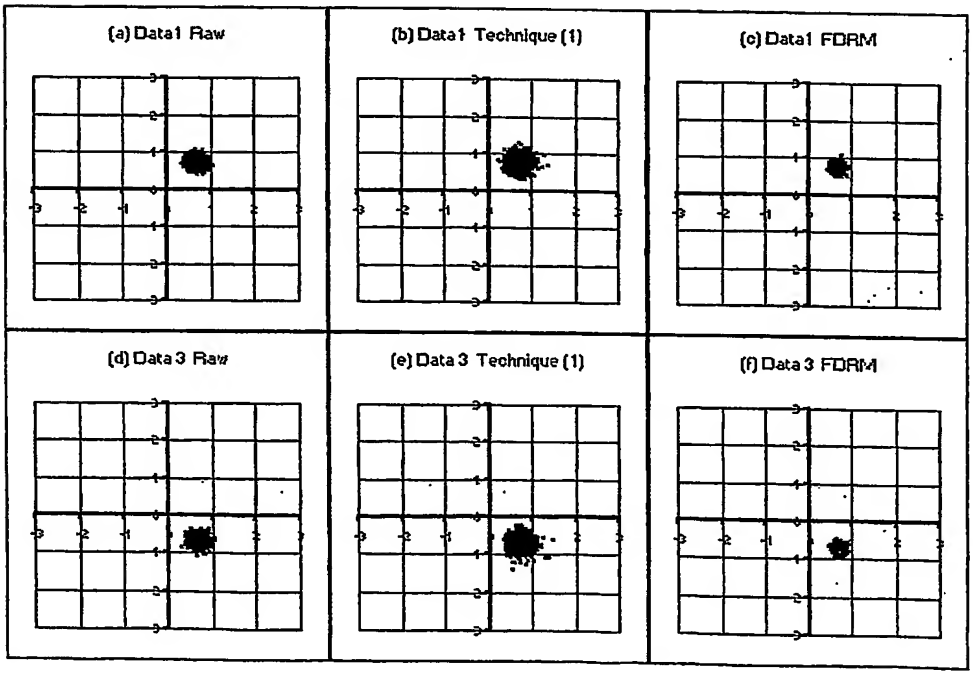

Figure 11

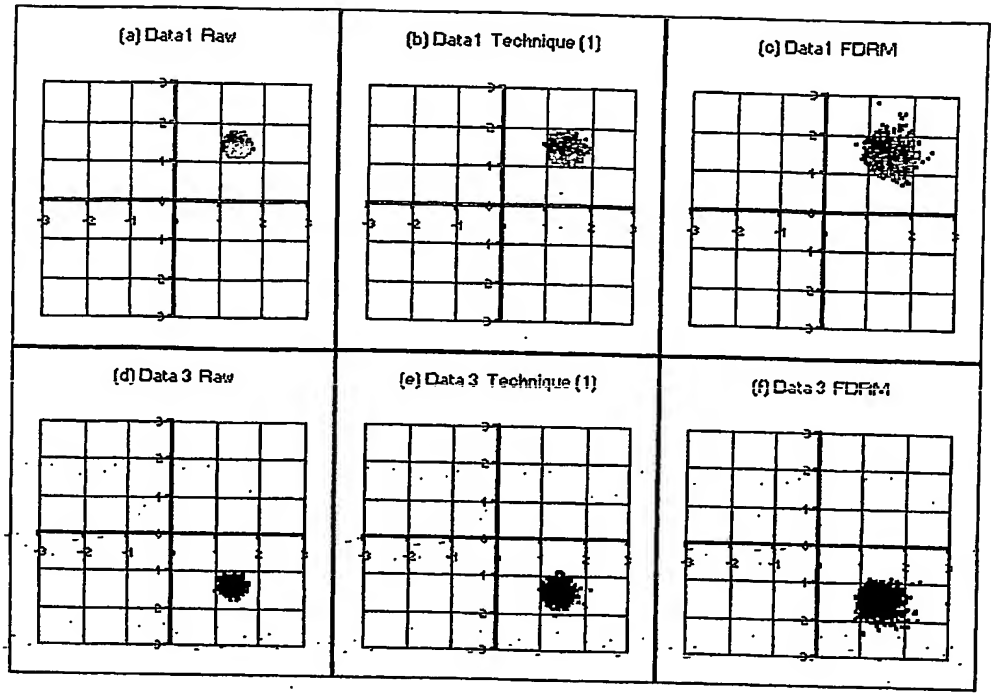

Figure 12

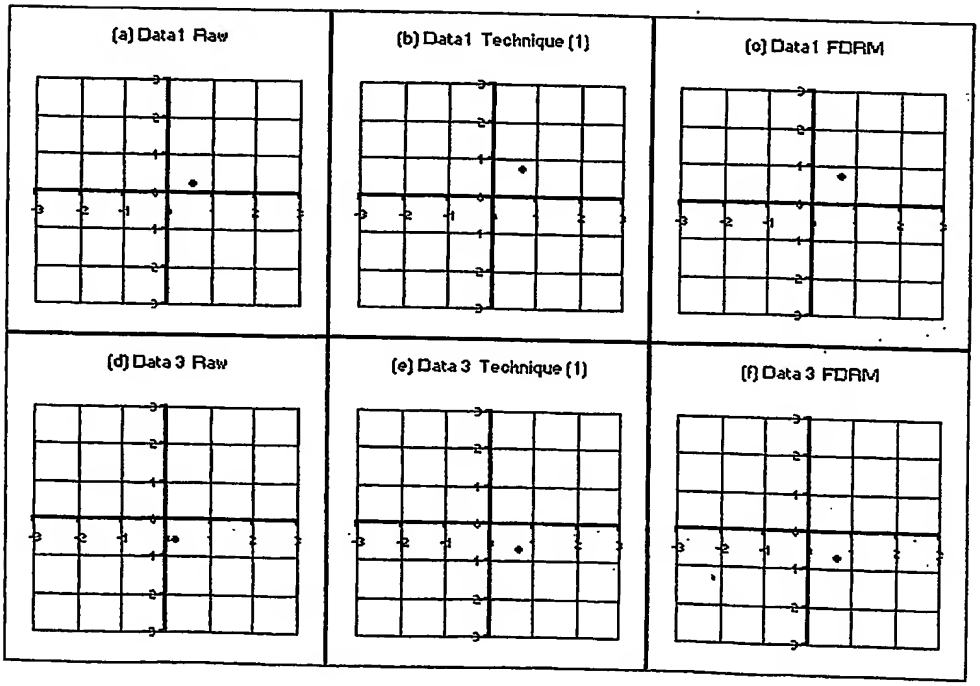

Figure 13

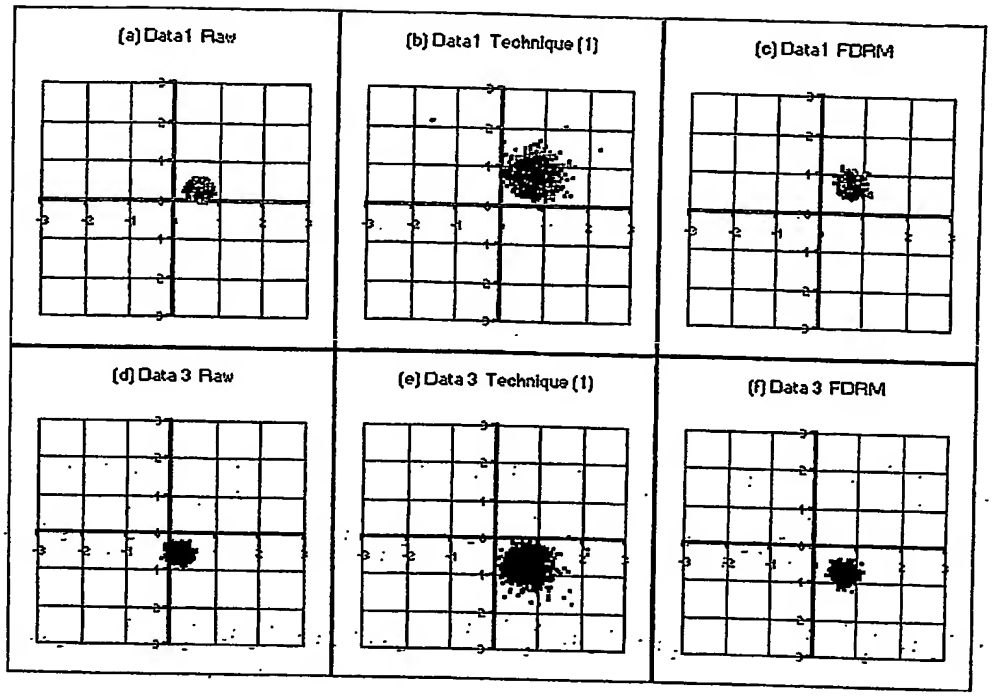

Figure 14

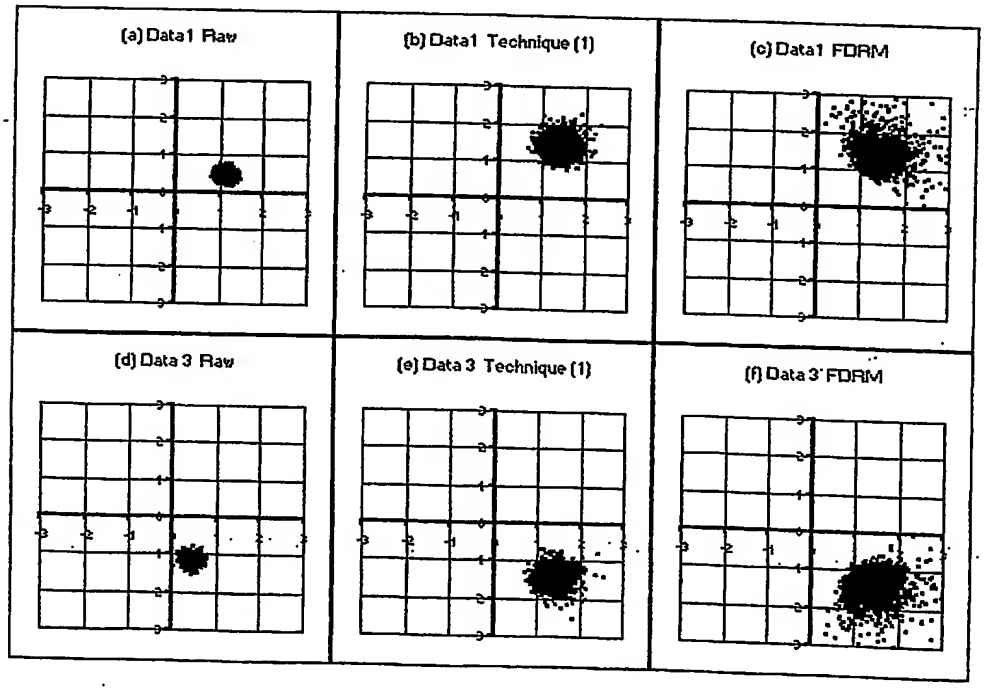

Figure 15

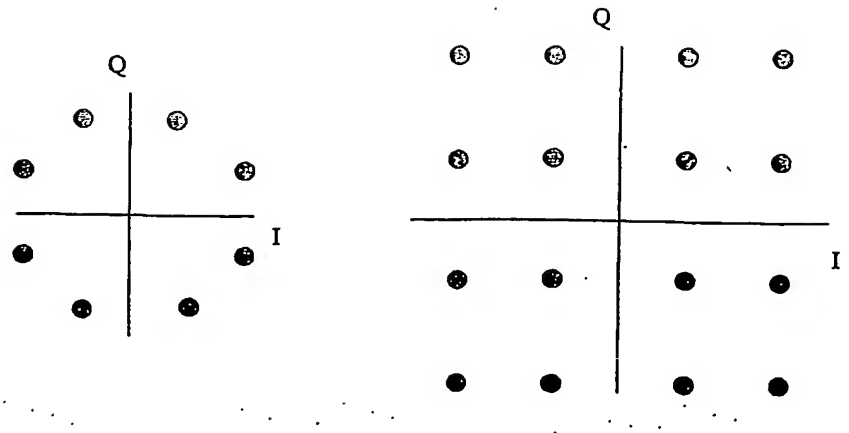

Figure 16

Data 1	Data 2	...	Data k	...	Data (N-1)	Data N

Figure 17

Data 1	Pilot Control Block Data 2	Data3

Figure 18

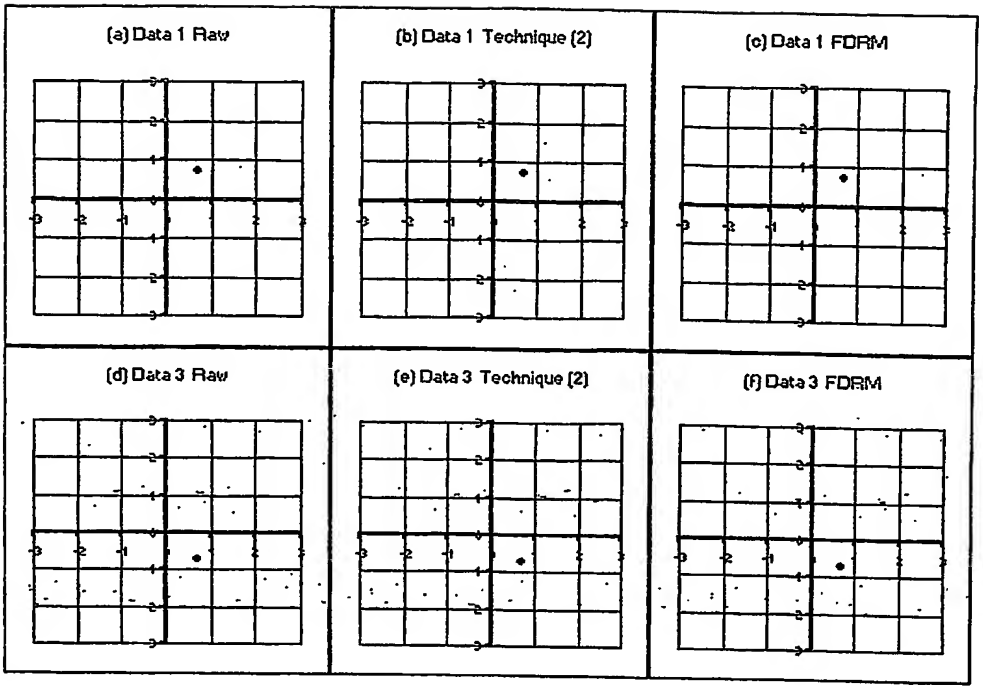

Figure 19

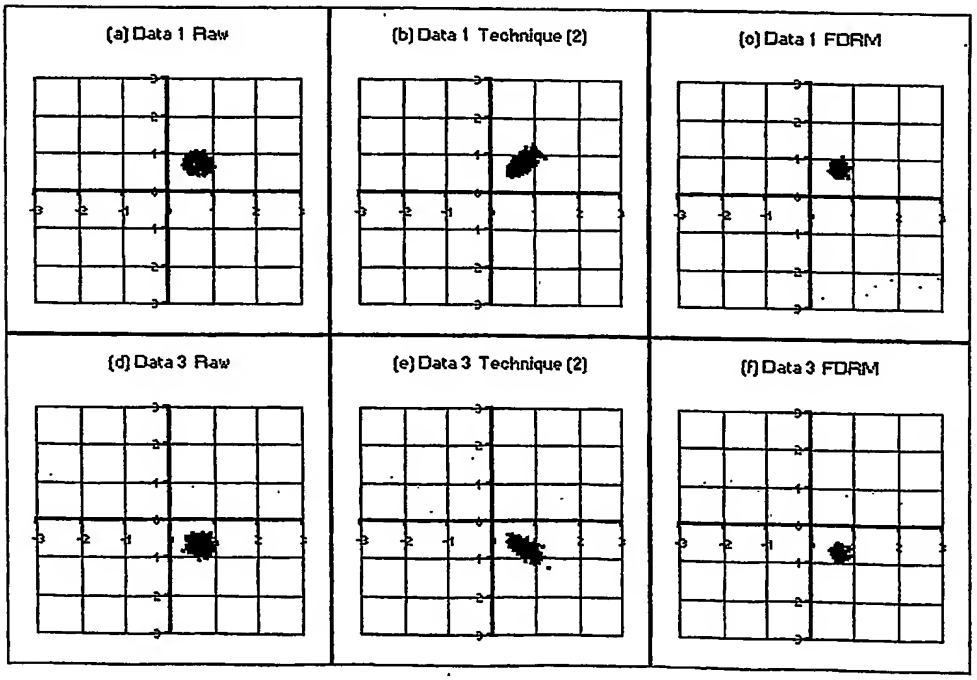

Figure 20

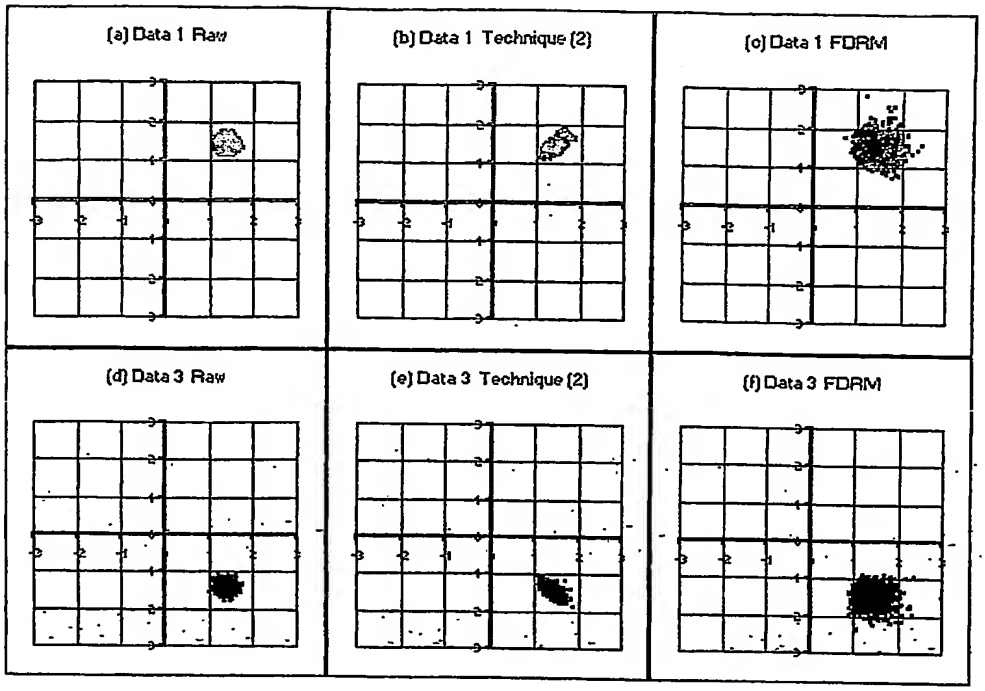

Figure 21

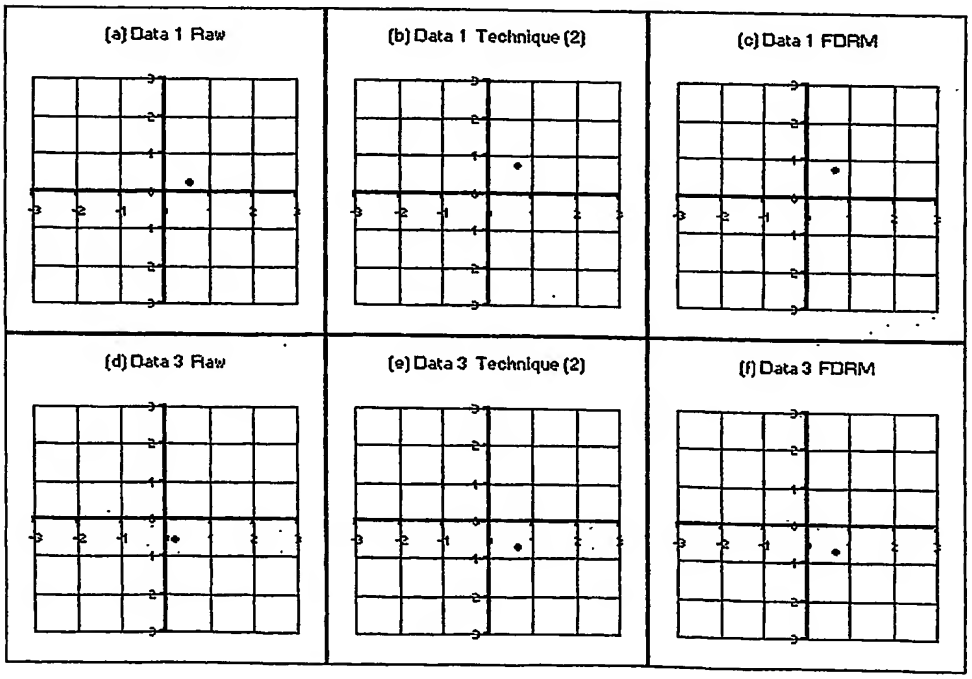

Figure 22

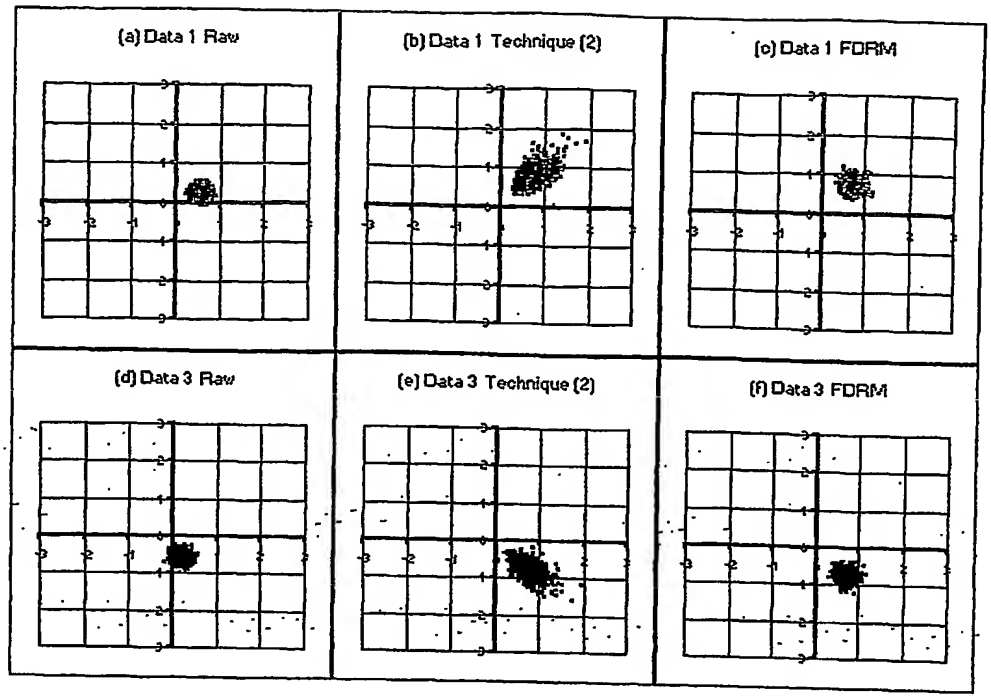

Figure 23

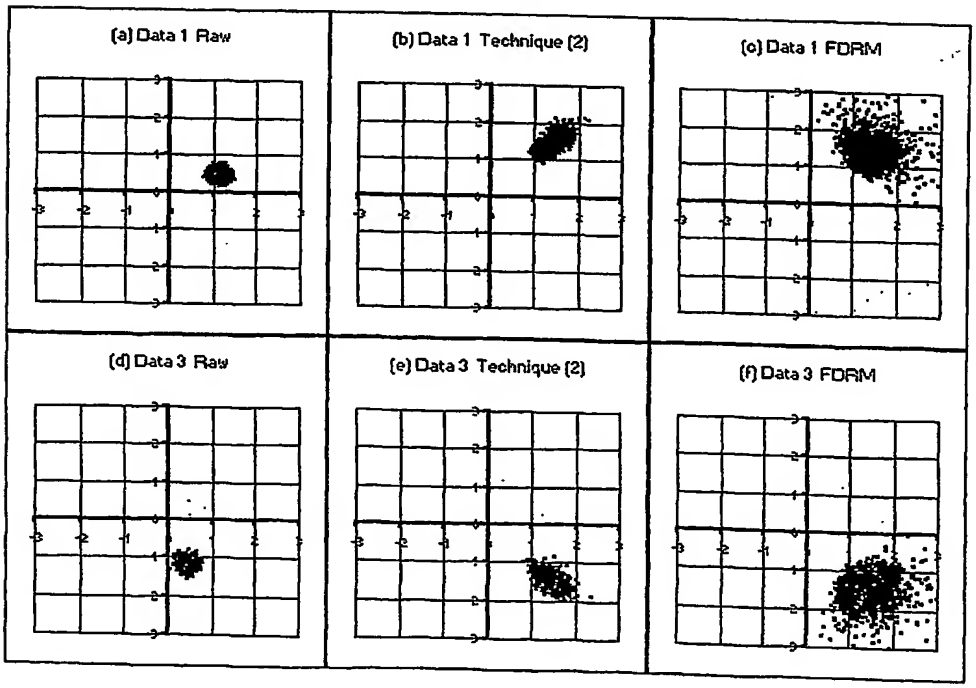

Figure 24

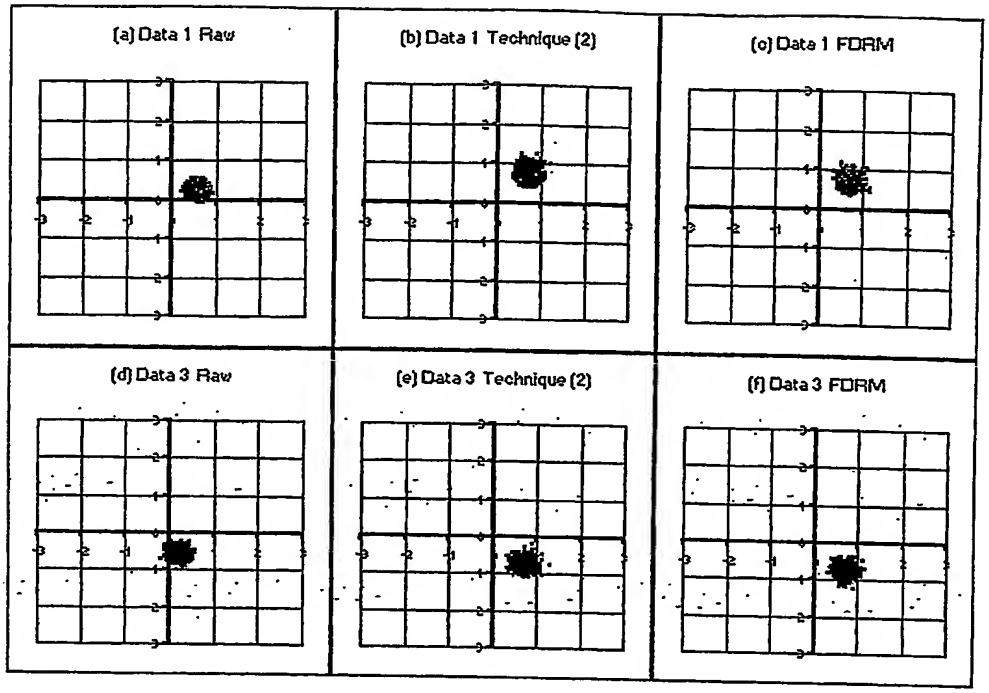

Figure 25

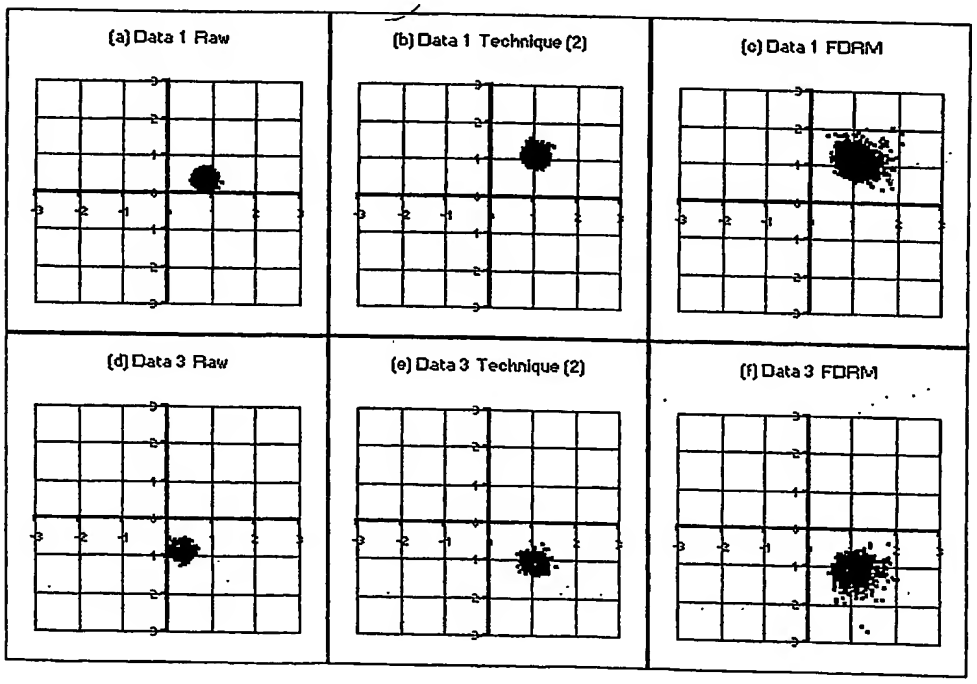

Figure 26

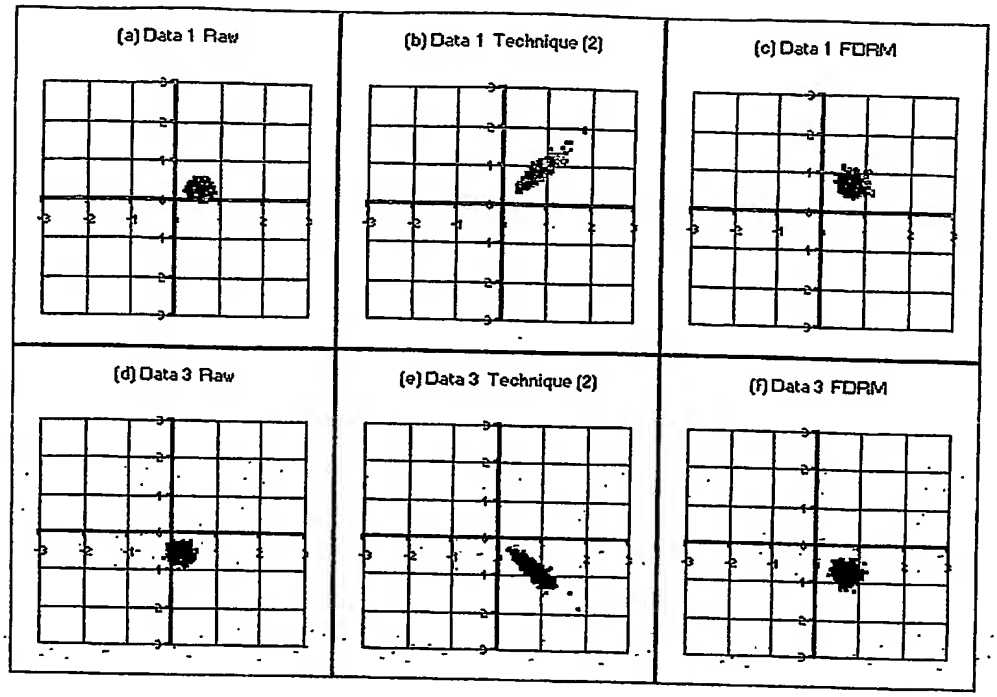

Figure 27

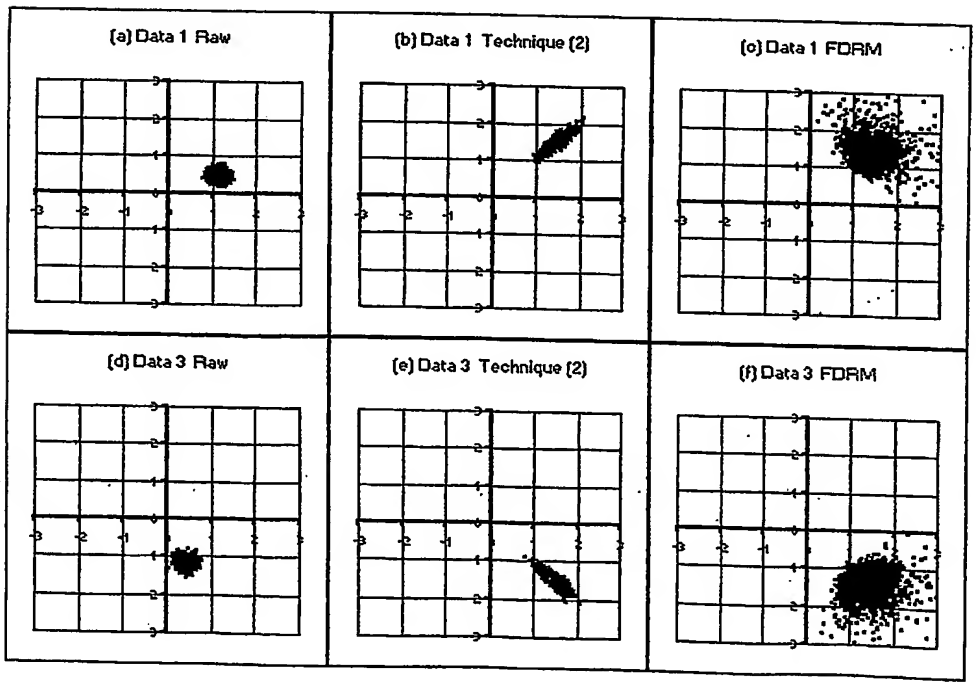

Figure 28

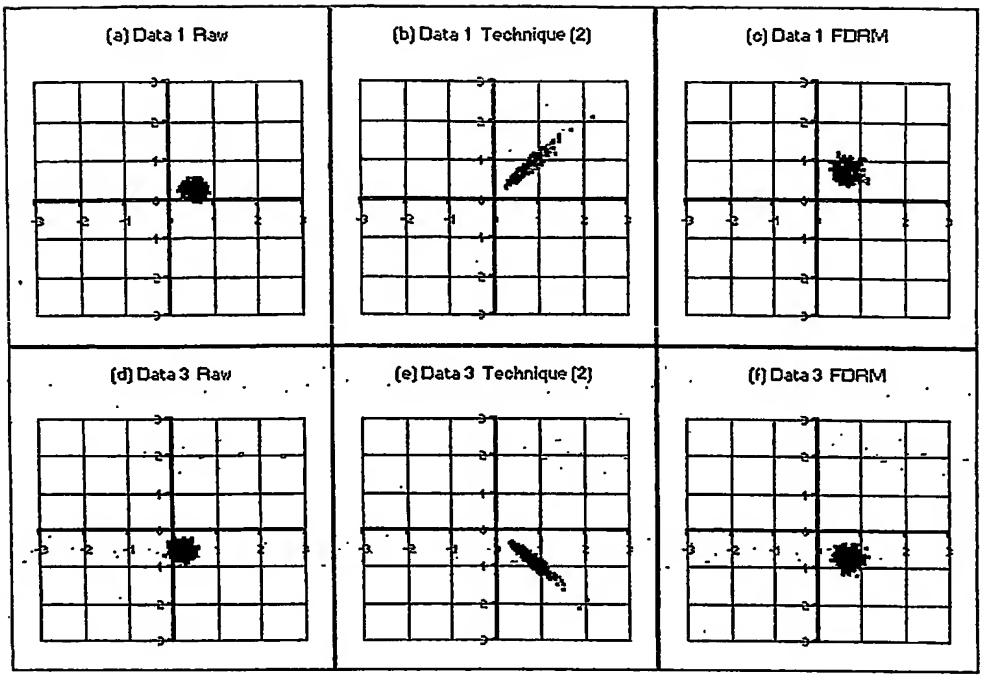

Figure 29

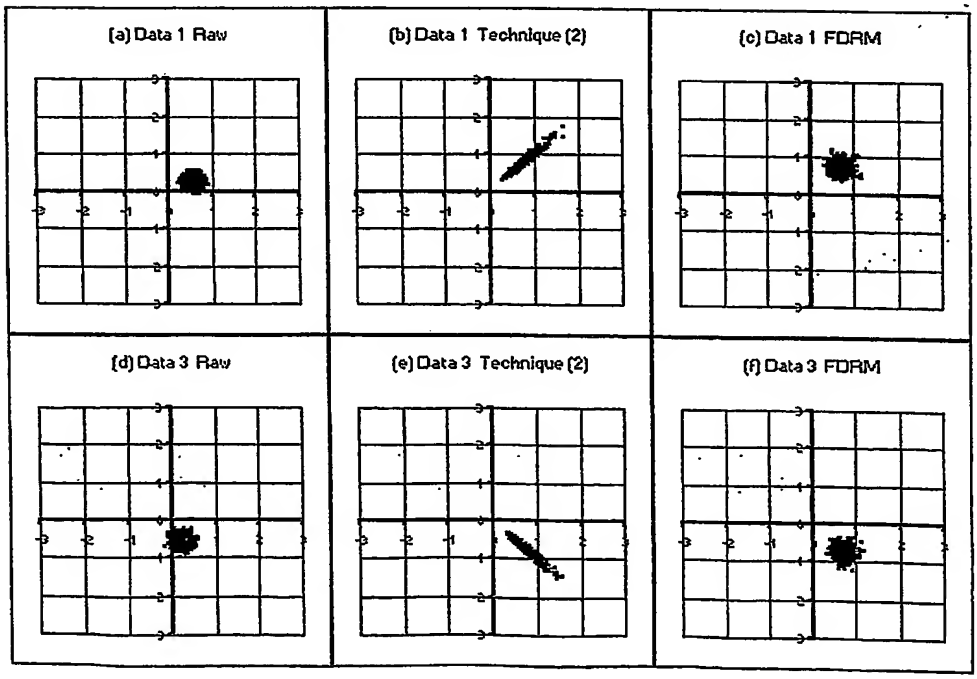

Figure 30

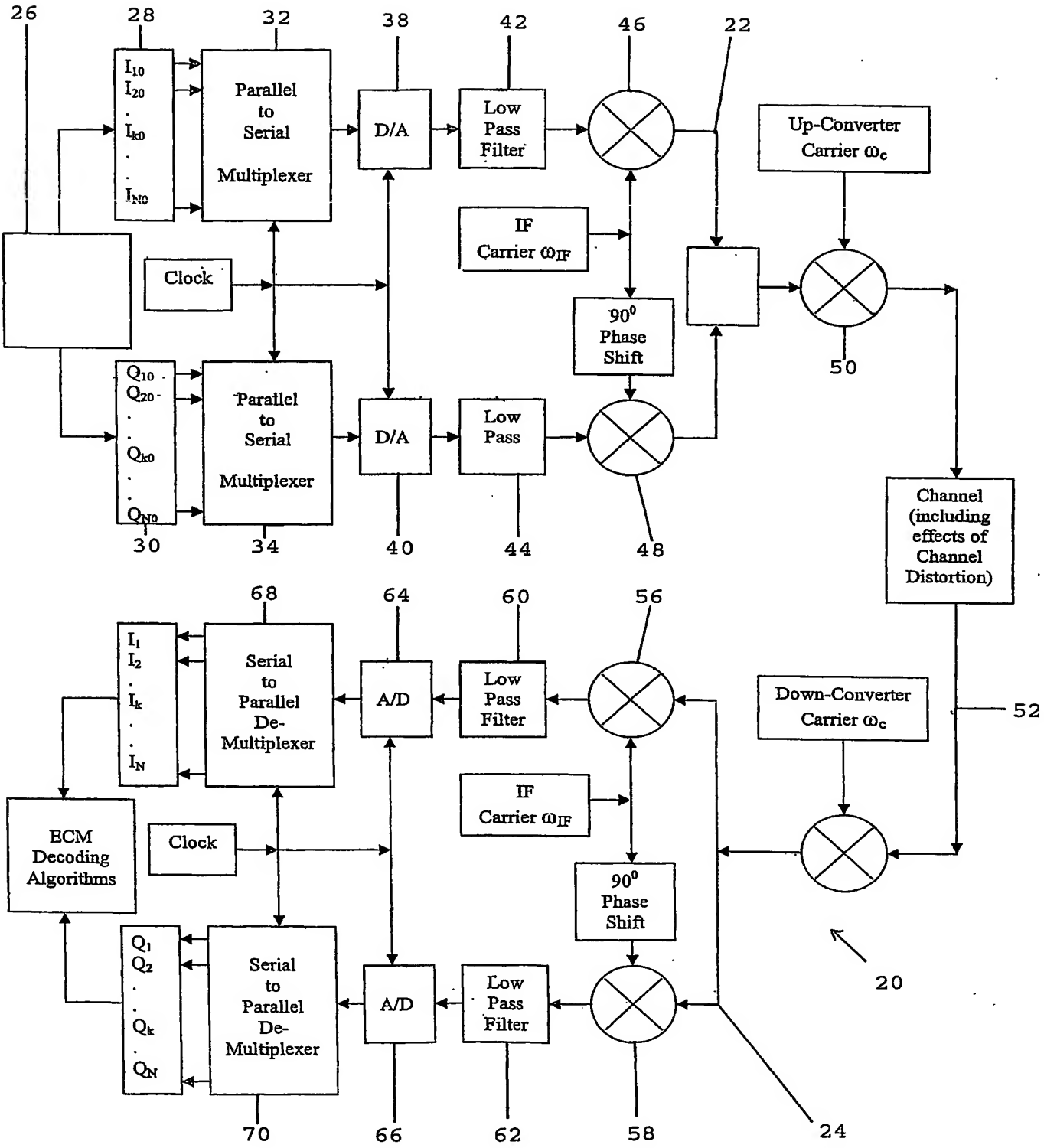
26
28
32
38
42
46
22
I_{10}
I_{20}
I_{k0}
I_{N0}
Parallel to Serial Multiplexer
D/A
Low Pass Filter
Up-Converter Carrier ω_c
IF Carrier ω_{IF}
Clock
90^0 Phase Shift
50
Q_{10}
Q_{20}
Q_{k0}
Q_{N0}
Parallel to Serial Multiplexer
D/A
Low Pass
Channel (including effects of Channel Distortion)
30
34
40
44
48
68
64
60
56
I_1
I_2
I_k
I_N
Serial to Parallel De-Multiplexer
A/D
Low Pass Filter
Down-Converter Carrier ω_c
52
IF Carrier ω_{IF}
ECM Decoding Algorithms
Clock
90^0 Phase Shift
20
Q_1
Q_2
Q_k
Q_N
Serial to Parallel De-Multiplexer
A/D
Low Pass Filter
70
66
62
58
24

Figure 31

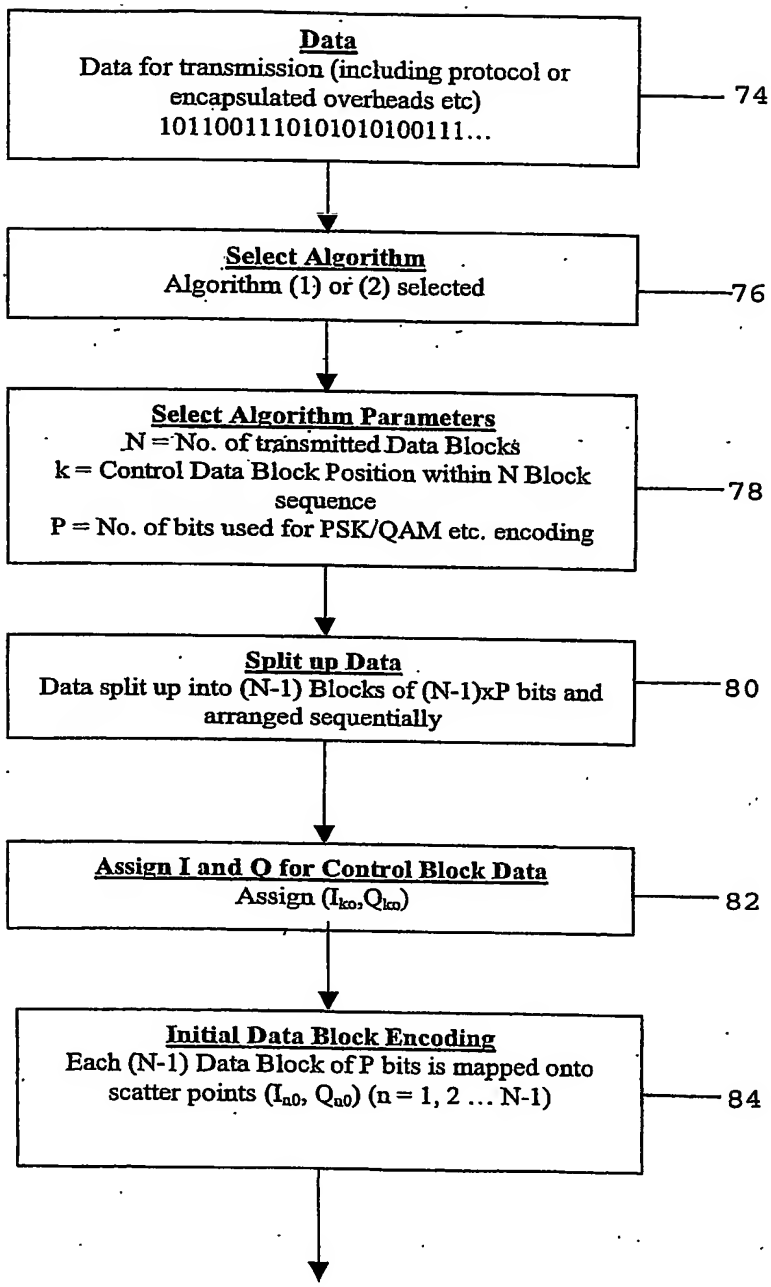
Data
Data for transmission (including protocol or encapsulated overheads etc)
101100111010101010100111...
74
Select Algorithm
Algorithm (1) or (2) selected
76
Select Algorithm Parameters
N = No. of transmitted Data Blocks
k = Control Data Block Position within N Block sequence
P = No. of bits used for PSK/QAM etc. encoding
78
Split up Data
Data split up into (N-1) Blocks of (N-1)xP bits and arranged sequentially
80
Assign I and Q for Control Block Data
Assign (I_{ko},Q_{ko})
82
Initial Data Block Encoding
Each (N-1) Data Block of P bits is mapped onto scatter points (I_{n0}, Q_{n0}) (n = 1, 2 ... N-1)
84

Figure 32

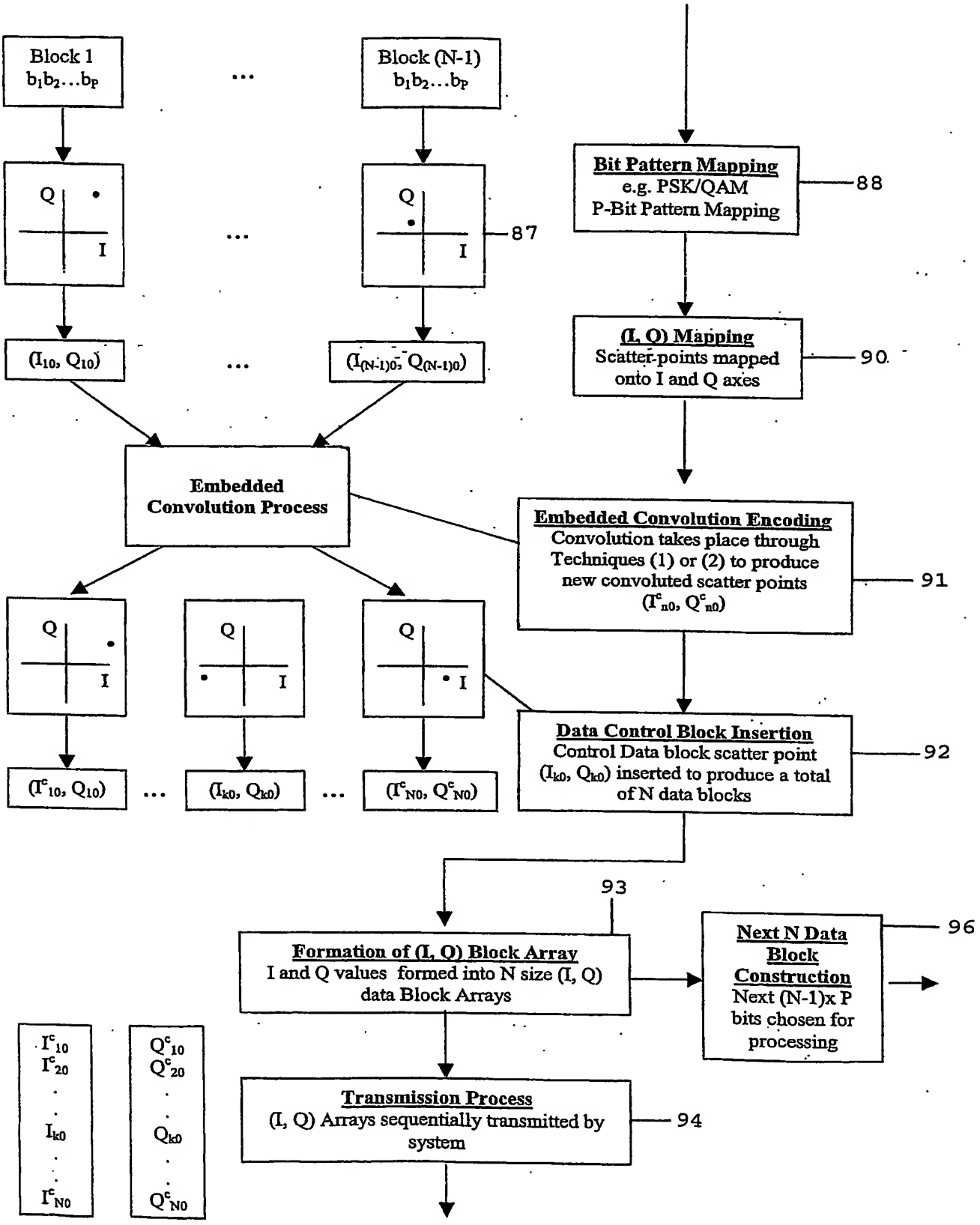

Figure 32 (Contd)

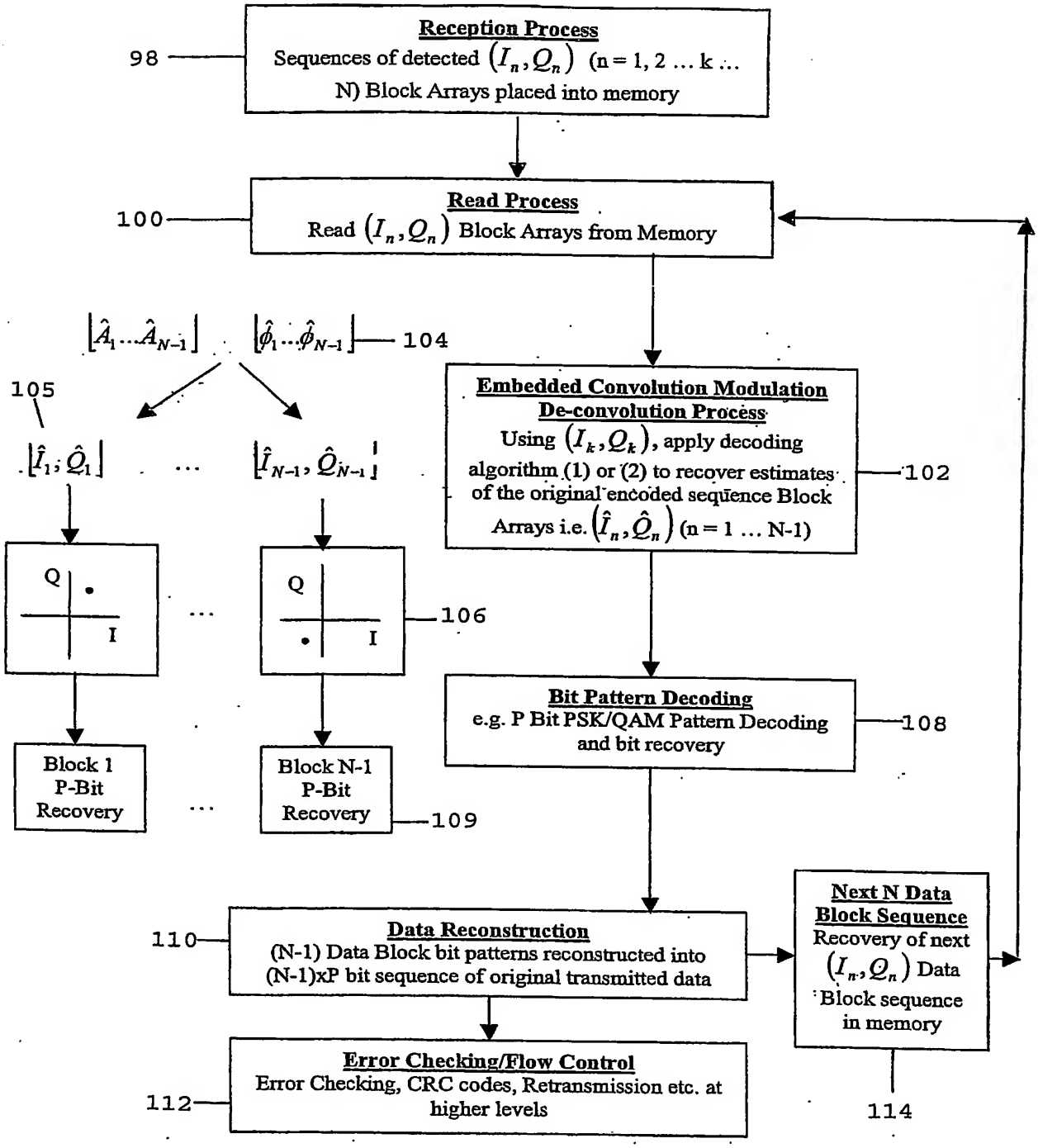
Reception Process
Sequences of detected (I_n, Q_n) (n = 1, 2 ... k ... N) Block Arrays placed into memory
98
Read Process
Read (I_n, Q_n) Block Arrays from Memory
100
$\hat{A}_1 \ldots \hat{A}_{N-1}$
$\hat{\phi}_1 \ldots \hat{\phi}_{N-1}$
104
105
$\hat{I}_1, \hat{Q}_1$
$\hat{I}_{N-1}, \hat{Q}_{N-1}$
Embedded Convolution Modulation De-convolution Process
Using (I_k, Q_k), apply decoding algorithm (1) or (2) to recover estimates of the original encoded sequence Block Arrays i.e. $(\hat{I}_n, \hat{Q}_n)$ (n = 1 ... N-1)
102
Q
I
106
Bit Pattern Decoding
e.g. P Bit PSK/QAM Pattern Decoding and bit recovery
108
Block 1 P-Bit Recovery
Block N-1 P-Bit Recovery
109
Data Reconstruction
(N-1) Data Block bit patterns reconstructed into (N-1)xP bit sequence of original transmitted data
110
Next N Data Block Sequence
Recovery of next (I_n, Q_n) Data Block sequence in memory
Error Checking/Flow Control
Error Checking, CRC codes, Retransmission etc. at higher levels
112
114

Figure 33

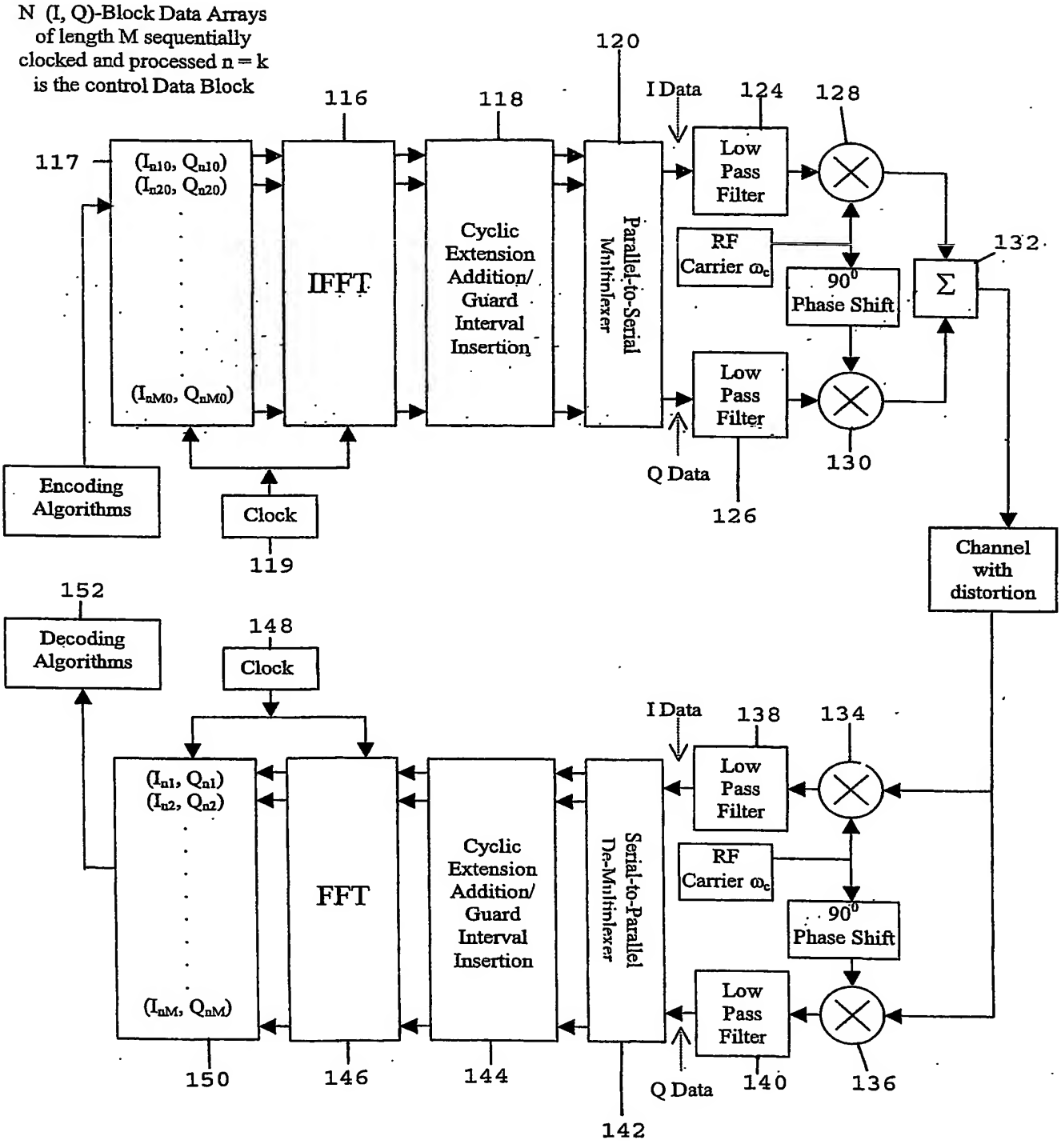
N (I, Q)-Block Data Arrays of length M sequentially clocked and processed n = k is the control Data Block
120
116
118
I Data
124
128
117
(I_{n10}, Q_{n10})
(I_{n20}, Q_{n20})
(I_{nM0}, Q_{nM0})
IFFT
Cyclic Extension Addition/ Guard Interval Insertion
Parallel-to-Serial Multiplexer
Low Pass Filter
RF Carrier ω_c
90^0 Phase Shift
Σ
132
Low Pass Filter
130
Q Data
126
Encoding Algorithms
Clock
119
Channel with distortion
152
Decoding Algorithms
148
Clock
I Data
138
134
(I_{n1}, Q_{n1})
(I_{n2}, Q_{n2})
(I_{nM}, Q_{nM})
FFT
Cyclic Extension Addition/ Guard Interval Insertion
Serial-to-Parallel De-Multiplexer
Low Pass Filter
RF Carrier ω_c
90^0 Phase Shift
Low Pass Filter
Q Data
140
136
150
146
144
142

Figure 34

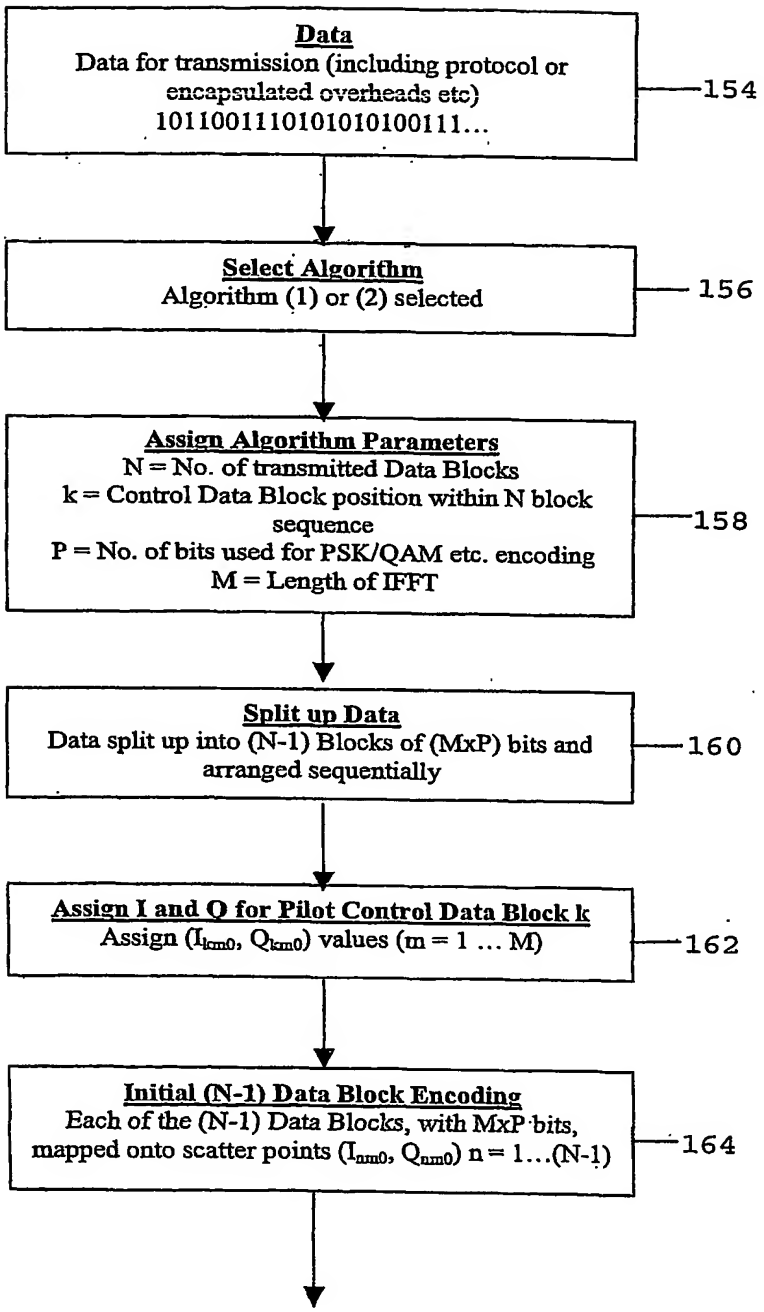
Data
Data for transmission (including protocol or encapsulated overheads etc)
10110011101010101001111...
154
Select Algorithm
Algorithm (1) or (2) selected
156
Assign Algorithm Parameters
N = No. of transmitted Data Blocks
k = Control Data Block position within N block sequence
P = No. of bits used for PSK/QAM etc. encoding
M = Length of IFFT
158
Split up Data
Data split up into (N-1) Blocks of (MxP) bits and arranged sequentially
160
Assign I and Q for Pilot Control Data Block k
Assign (I_{km0}, Q_{km0}) values (m = 1 ... M)
162
Initial (N-1) Data Block Encoding
Each of the (N-1) Data Blocks, with MxP bits, mapped onto scatter points (I_{nm0}, Q_{nm0}) n = 1...(N-1)
164

Figure 35

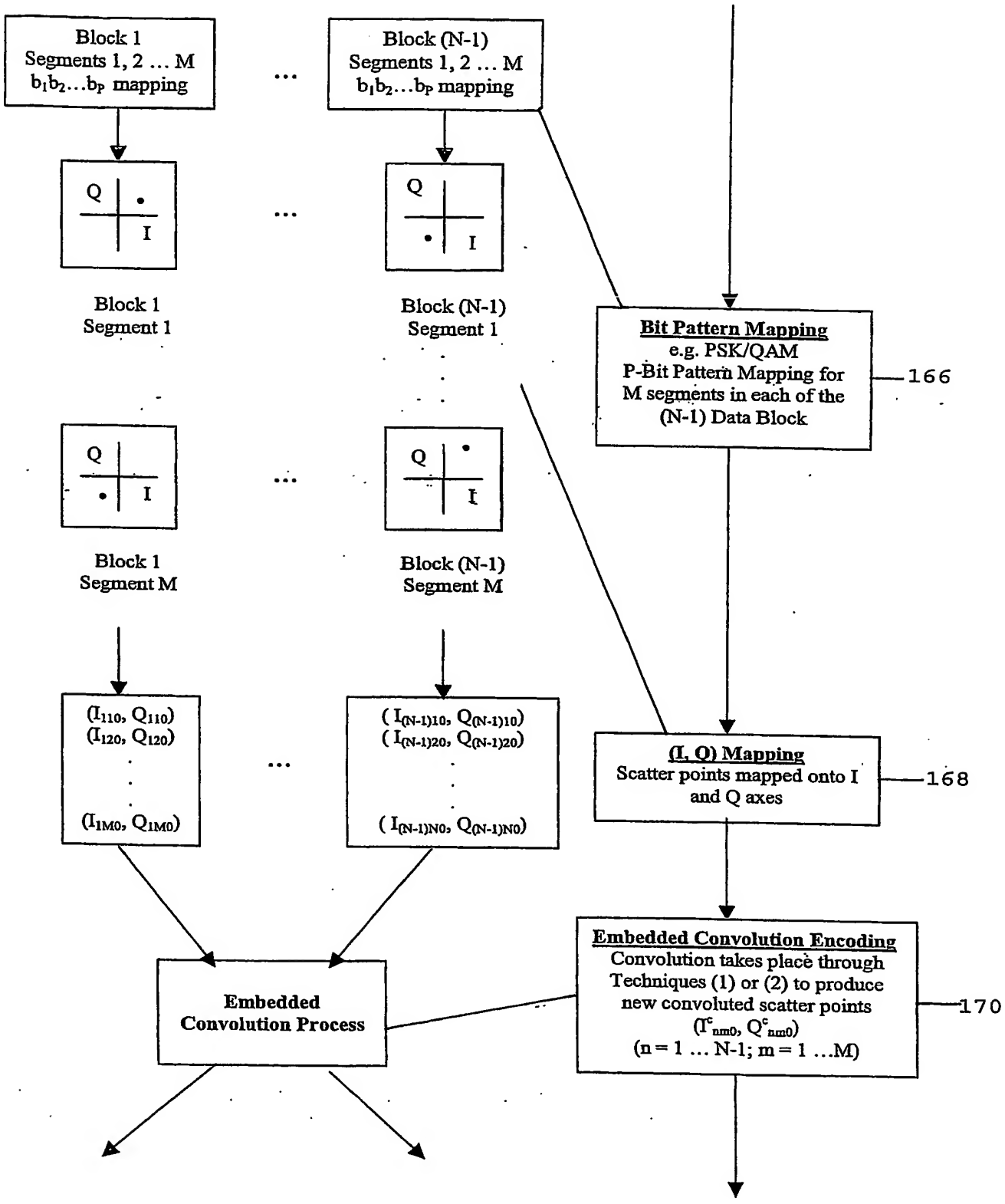

Figure 35 (Contd)

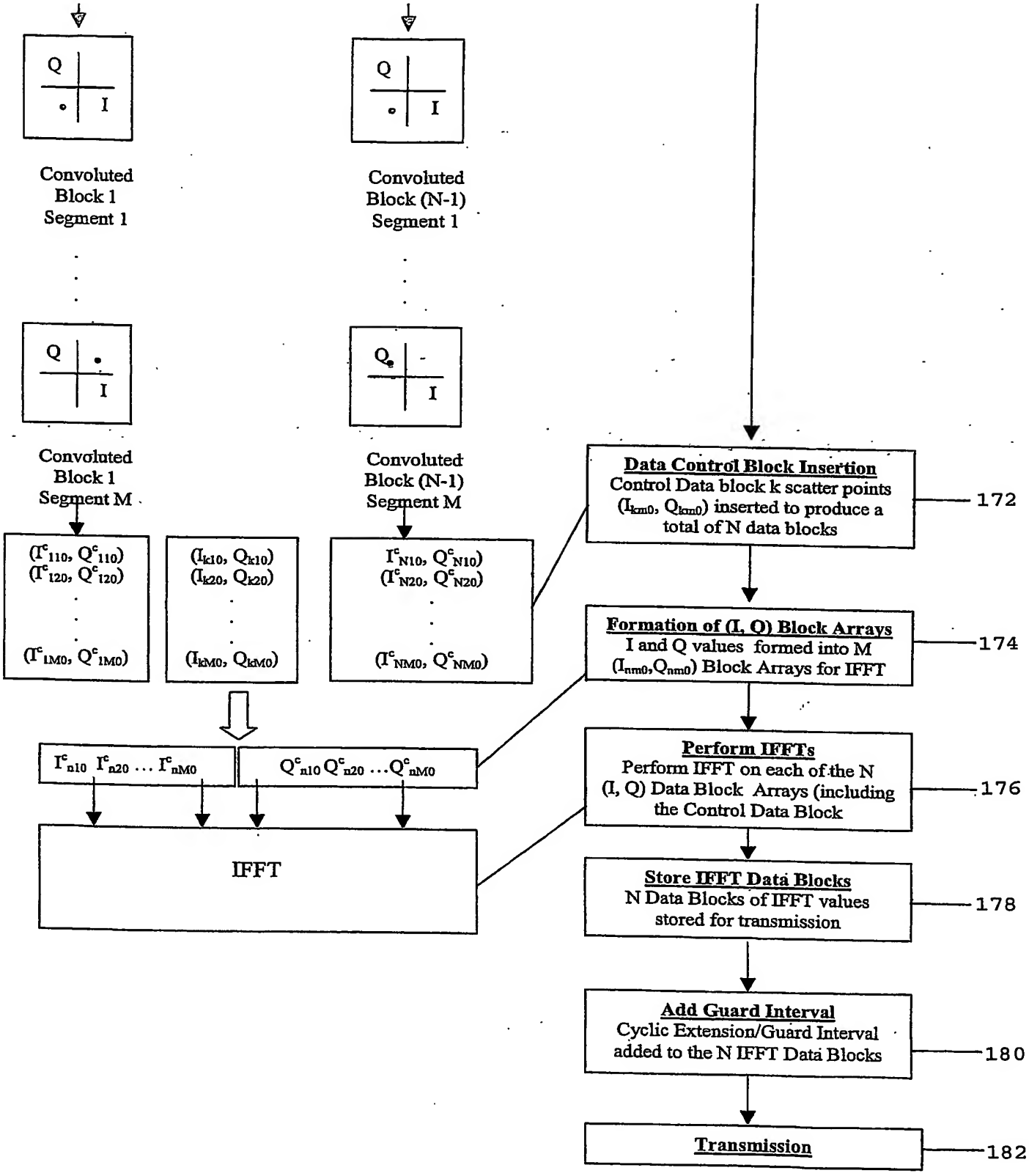

Figure 35 (Contd)

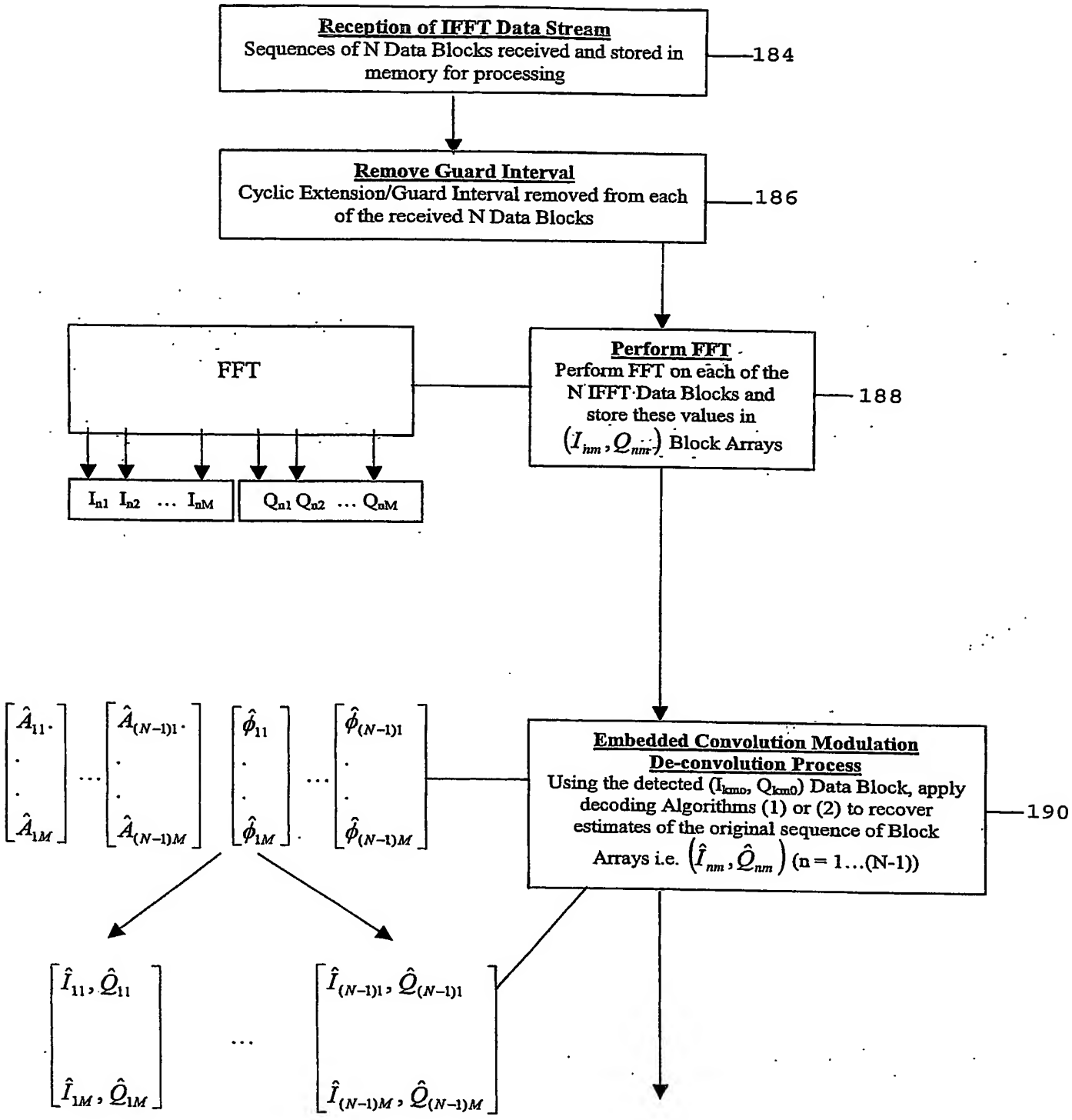
Reception of IFFT Data Stream
Sequences of N Data Blocks received and stored in memory for processing
184
Remove Guard Interval
Cyclic Extension/Guard Interval removed from each of the received N Data Blocks
186
FFT
Perform FFT
Perform FFT on each of the N IFFT Data Blocks and store these values in (I_{nm}, Q_{nm}) Block Arrays
188
I_{n1} I_{n2} … I_{nM}
Q_{n1} Q_{n2} … Q_{nM}
$\hat{A}_{11}$ … $\hat{A}_{1M}$
$\hat{A}_{(N-1)1}$ … $\hat{A}_{(N-1)M}$
$\hat{\phi}_{11}$ … $\hat{\phi}_{1M}$
$\hat{\phi}_{(N-1)1}$ … $\hat{\phi}_{(N-1)M}$
Embedded Convolution Modulation De-convolution Process
Using the detected (I_{kmo}, Q_{km0}) Data Block, apply decoding Algorithms (1) or (2) to recover estimates of the original sequence of Block Arrays i.e. $(\hat{I}_{nm}, \hat{Q}_{nm})$ (n = 1…(N-1))
190
$\hat{I}_{11}, \hat{Q}_{11}$
$\hat{I}_{1M}, \hat{Q}_{1M}$
$\hat{I}_{(N-1)1}, \hat{Q}_{(N-1)1}$
$\hat{I}_{(N-1)M}, \hat{Q}_{(N-1)M}$

Figure 36

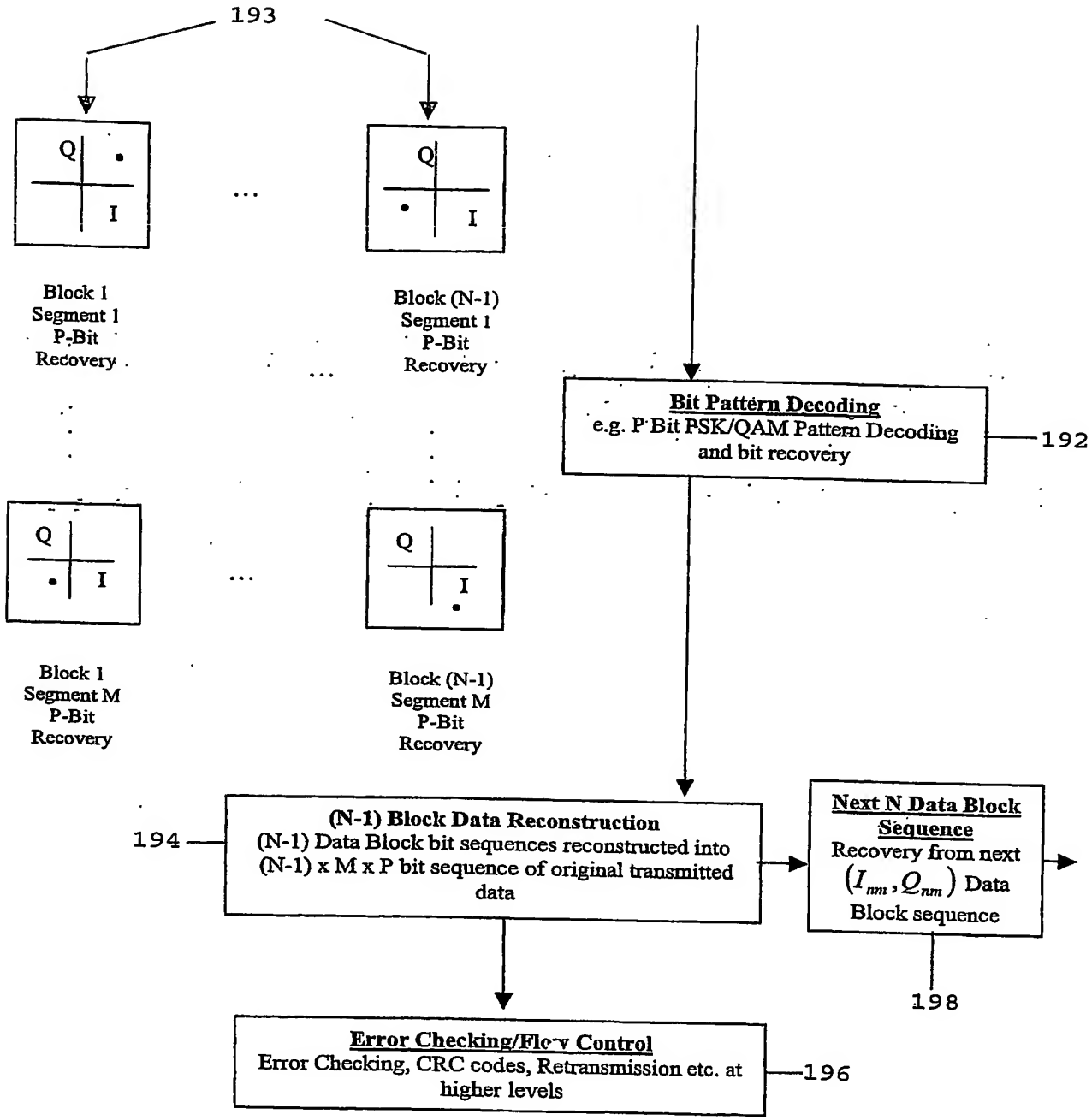

Figure 36 (Contd)